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D/Craig
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Kedo et al.

Serial No.: 09/872,007 **Group Art Unit:** 2822

Filed: June 04, 2001 **Examiner:** Soward, Ida M.

For: FABRICATION OF LOW POWER CMOS DEVICE WITH HIGH RELIABILITY

Honorable Commissioner of Patents
Washington, D.C. 20231

AMENDMENT UNDER 37 C.F.R. §1.111

Sir:

In response to the Office Action dated February 27, 2002, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend claims 3-4 and add new claims 18- 19 as follows:

3. (Amended) A method for fabricating on a semiconductor substrate a semiconductor device, the method comprising:

forming an isolation region within a semiconductor substrate and close to a surface of the semiconductor substrate to define a first region for a first gate oxide film of a first MOSFET and a second region for second and third MOSFETs;

selectively implanting fluorine ions into a first part of the second region with a first ion-implantation condition, the first part of the second region being for the second MOSFET, the first ion-implantation condition being determined to form a second gate oxide film;